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Summary Experience and Areas of interested Growth

Over 25 years as a test technologist focused on mixed-signal and analog test methods. Effectively proves new test methods which impact manufacturing test with empirical data and drives adoption via presentations, documentation and training. Known for extraordinary collaboration skills- connecting people and connecting knowledge across engineering teams. Looking for a position which would take advantage technical leadership and further develop data analytic skills.

Professional Experience

Intel SVE/EV; Electrical Validationn(EV) Engineer Aug 2013 to July 2015

- Ramped up on EV methodologies to support liason to Manufacturing Development Organinzation (MDO) analog partners. Created a fishbone diagram which captured factors impacting correlation between EV and MDO measurements. Lead an engineering team to define a Converged Unit Selection Methodology to support Electrical Validation, Bench-level Circuit evaluation and Manufacturing Test Design Validation. Results: standard forum-Product Process Interaction Team (P.P.I.T.) and technical process for using carefully selected units (SMart Unit Gleaning).
- Led a 14nm SoC product P.P.I.T. and executed Material Analyst role for SMUG A-step parts. Selected a software tool from available options which enabled improved support. Ramped up on software tool, gave constant feedback to developers to improve tool, worked with New Product Planner to make sure units could be selected in a timely fashion. Work recognized with a Q1 2015 Division recognition award.
- Contributed to Lab Efficiency Team's strategic vision of data system tool integration for non-manufcturing labs (~1,500 labs, square feet half of the a modern fab and 2+ billion dollars in assets). Determined that effort needed extensive interviews with key customers, lab nanagers and Information Quality Surveys on key databases. Leveraged knowledge experts on user experience and ethnogrophy to develop questions and personal interviewed 19 lab managers resulting in 40 hours to analyze. Led Information Quality Surveys on 3 key data systems and in process trained another team member how to do this. Summarized findings and presented to Lab Efficiency Team and program mangers.

Intel STTD; Test R&D Engineer Feb 1994 to Aug 2013

- Jan 2011- Nov 2013: Conceived notion of tracking IP HVM performance to support Intel's SoC products. Gathered experts to define it and executed a proof of concept on 32nm products. POC confirmed that with appropriate DFT architecture can easily support identifying failing IP and identified acquiring the IP design data as in issue. Pilot on 22 nm product done which highlighted challenges in mapping the IP design data to the test of the IP.

- Dec 2008- Aug 2013: Tooling and DFT Technology working group leader, WG develops and promotes DFT test methods which support simpler load board designs. With NTT WG members made a strong case for the No Touch Test (NTT) methods that would support increasing parallel test on future CPUs for 22nm. Directed execution of experiments on new and existing No Touch Leakage methods. Led WG to document current tooling configurations and implementation trends for unit and wafer level test. WG currently focused on comprehending total cost ownership.
- June 2009-Aug 2014: Conceived a monthly forum for sharing tips and ideas on technical leadership which also fosters informal networking. The Oregon Technical Leadership Forum has successfully hosted 10 monthly forums for 5 years and has a mailing list > 450 names.
- Jan 2008-Aug 2013: Garnered internal support for Intel funding academic research in PLL DFX. Led a 4 year relationship via monthly meetings between Intel engineers and research group which resulted in a summer 2011 internship to investigate using the developed DFX methods on Intel processes. Results shared at 2012 internal conference. Defined a test chip experiment, secured the mask designers for layout and personally supported circuit schematics for 22nm process. Relationship has resulted in two PhD students (one hired at Intel), numerous external papers, and Intel access to developed IP.
- Dec 2006-Nov 2008: Participated in SOC DFT & HVM WG and drove Analog/IO Testing strategy. Collaborated with Hard IP DFX engineers to develop IO DFX standardization, which addressed test infrastructure, basic requirements and identified need for additional DFX team members and back-end PDE support. Conducted an extensive competitive analysis on IO and Analog test within SOCs.
- March 2005- 2008: Led development of two courses on Intel IO DFT based test methods (Basics and Theory and Practice) by forming an instructor team. Major update of material made in 2008. Supported creating Web Based Training of Basics class. Trained additional instructors and personally have given training to 100's of engineers.
- Jan 2005-Nov 2006: Identified Key HSIO RX circuitry that required additional path finding- RX equalization and RX Data Clock Recovery. Projects defined and directed engineers to complete the study with recommendations. Jitter test gap investigation identified small gaps and recommended test coverage strategies. RX equalization test gap project resulted in two methodologies developed and documented.
- Sept 2004- Oct 2006: Influenced DFT definition for QPI and FBD HSIOs by documenting requirements in QPI spec and FBD design guide. Drove IO DFX direction of CPU uncore tech readiness by revising IO DFX features for QPI/FBD and sideband signals and writing high level architectural spec on structural test and loopback modes. Defined and directed DFT implementation for QPI on test chip. DFT included slow speed operation and no-touch test leakage. Developed QPI Interface requirement for ATE vendors.
- Jan 2003-Dec 2005: Led STTD early engagement for HSIO test method development by executing and guiding Inductive Fault Analysis (IFA) on key circuits. Worked with 3GIO DFT WG on defining DFT requirements, and directing Pre-Si DFT for PCI Express and Scidlink MI. Effort identified issues, work-arounds and improvements. Results communicated to Test engineer, DFT and IO design communities via presentation and documentation.
- Jan 1997-Dec 2002: Validated AC IO Loopback DFT on WMT, 1st CPU to use this method. Analyzed AC IO loopback silicon data and provided input to establish fail limits. Chaired 858.2 IO Test WG which supported all the Defect Based IO Tests. Used this group to drive silicon fixes to fully enable AC IO loopback. Proliferated the methodology via

documentation and training. This technology continues to be used on nearly all Intel single-ended interfaces, i.e. DDR.

- Feb 1994-Dec 1996: Designed 1st Weak Write Test Mode (WWTM) circuit deployed on a P854 CPU. Developed qualification plan, performed data analysis from test programs and failure characterization, and proliferated the method via internal conference papers, internal documentation and training presentation. WWTM substituted the data retention test which significantly impacted test time (~100 us vs 1 sec). Technology successfully used for over 10 years.

Carnegie Mellon University, Department of Electrical and Computer Engineering; Research Assistant, August 1988- Dec 1993

Developed a general methodology for analog fault model development, implemented for CMOS opamps. Designed op amps covering a range of topologies. Evaluated the effects of shorts on CMOS op amp behaviors. Developed PERL code to post-process results and created circuit simulation input files for further analysis. Developed series of simulation experiments to determine resulting fault behaviors.

IBM East Fish Kill NY; Associate Engineer, March 1985- August 1988

Performance evaluation of logic gate array designs for high end computers. Evaluated via empirical experiments first Weighted Random Pattern test application at IBM (Pre-cursor to Logic BIST using weighted random patterns.)

PATENTS, AWARDS AND PUBLICATIONS

PATENTS

- Patent # 5,559,145 "Static Random Access Memory SRAM Having Weak Write Test Circuit"
- Patent # 6,477,674, "Method and Apparatus for Conducting Input/Output Loop Back Tests Using a Local Pattern Generator and Delay Elements"
- Patent # 7,019,550, "Leakage Testing For Differential Signal Transceiver"

AWARDS

- 2003 International Test Conference Best Paper
- 2002 Best Intel Intern Manager Award
- 2001 Intel Design and Test Technology Conference Best Paper
- 1999 Intel Volunteer of the Year
- 1995 Intel Design and Test Technology Conference Best Written Paper
- 1996 International Test Conference Best Paper

PUBLICATIONS

- 12 external publications, presentations or posters, 5 most recent below.
- 2013 VLSI Test Symposium: "Universal IDDQ BIST for Analog/Mixed-Signal Macros with a Phase-Locked Loop Application."
- 2012 Design and Technology of Integrated Systems Conference: "Improving IO Test and System Evaluation via Data Sharing."
- 2011 VLSI Test Symposium : "Challenges in High Volume Manufacturing Test of HSIO and Correlation to System Performance" invited industrial talk

- 2011 VLSI Test Symposium: “An Industrial Case Study of Analog Fault Modeling “
- 2008 International Test Conference, “External Loopback Testing Experiences with High Speed Serial Interfaces”
- > 10 internal publications, presentations at Intel Conferences

PARTICIPATION IN TECHNICAL ACTIVITIES

- IEEE Member since 1994; International Test Conference Program Committee 2000-2004
- SRC Liaison for Prof Sule Ozev, Duke University than Arizona State University on analog fault modeling methods for test coverage and yield estimation- 2004-2010
- Intel Research Liaison for Prof Martin Margala, University of Massachusetts Lowell on PLL DFX research
- Reviewer for IEEE test conferences and publications and internal Intel conferences

Education

Carnegie Mellon University (Pittsburgh PA); PhD in Electrical and Computer Engineering

Polytechnic University (New York, NY, note now merged with New York Univeristy); MS Electrical Engineering

University of Maryland (College Park, MD); BS Electrical Engineering

RELEVENT OTHER EXPERIENCE

- Professional Ski Instructor of America (PSIA) for 19 winter seasons at Mt Hood Meadows. Certifications in childrens and senior teaching. Certification level II Alpine.
- Hollywood Farmers Market volunteer since 1997: responsibilities include greeter, crowd counts, assist single vendors on an as needed basis.
- St Mary Magdelene Parish- Chair of Hospitality Committee from 2008-2013: took an adhoc process for volunteers to support Sunday Coffee and Donuts after Mass Fellowship and created a streamlined process which increased volunteer ease and improved business relationship with local Alberstons from whom donuts were ordered.