Improved Understanding of IP Manufacturability—A Proposal to Share Data between Fab, Test and Design

Anne Meixner PhD

The Engineers' Daughter LLC
Portland, OR USA
anne.meixner@alumni.cmu.edu

***Abstract*—The semiconductor industry has knowledge siloed into Design, Fab and Test. This paper proposes data structures specific to IP design characteristics for test manufacturing data system that can connect these silos. These structures enhance the ability to comprehend manufacturability at the IP level. Benefits for IDMs, Foundries, IP developers and System on a Chip (SoC) design houses are listed. Challenges in implementing these data structures in an IDM environment are included as well as data analysis examples.**

Keywords—Yield, IP block, Circuit Design parameters, improved yield

I. Connecting Knowledge Silos

System on a Chip (SoC) design style has resulted in more rapid design of IC products and fostered the Foundry/Fabless eco-system. The SoC plug and play design style has not, anecdotally, translated into faster product ramping. Intellectual Property (IP) reuse ranges from 44% to 73% [1][2], hence; other barriers have impeded faster product ramping. Semiconductor knowledge is siloed into IP/SoC Design, Fab, Test (see Figure 1). Both Integrated Device Manufacturers (IDMs) and the Foundry eco-system continue to suffer from lack of connections between these silos. This paper proposes connecting the knowledge silos by monitoring IP failures and by providing relevant IP design data. Engineering organizations benefit from reduced engineering activities and increased understanding of IP manufacturability (yield related to pass/fail and performance).

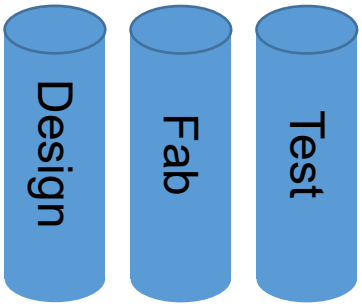

Figure 1 Product Knowledge Silos

The following scenario illustrates the impact accurate information can have on engineering time expended on a yield issue. After ramping in the Development Fab the StarLilly product has been transferred to Fab15. A yield issue occurs and is isolated to IPblock 546. The Fab15 data shows a correlation between IPblock 546 and NMOS1 device type. Weeks go by with tweaks to the process and no change to the yield issue, nor the correlation. Jayne, a senior product engineer, spent hundreds of hours of her own time examining all **available** data. Frustrated she contacts Paul, her peer at the Development Fab, who informs her device NMOS1 type is not in IPblock 546 but NMOSL, NN1, PMOSL, and PP1 are included [3]. Paul had the design info in his head as a result from working with designers during the initial ramp. Jayne fell victim to a *spurious correlation* [4]. For real time understanding she required some essential design data that would have prevented her wild goose chase.

Understanding the IP performance within a production manufacturing environment has a number of benefits that are currently not enabled. The SoC model requires silicon proven IP for Hard IP and often Soft IP developers demonstrate IP in silicon. A test chip of an IP authenticates performance specifications and to first order proves production worthiness. However, with today's advanced process nodes and chip complexities, the intricacies of design-process interactions cannot be fully understood with test chips [5][6][7]. Production data for an IP can show how those subtleties will manifest, be it device performance over a wafer, layout specific structures or IP block placement.

In today's semiconductor wafer/unit test programs failing behavior in the form of hard and soft bins indicates how a part fails and may imply where. For instance, Memory and logic failures are easily separated by hard bins. Because there exist no standards for bin-naming, test engineers are unable to track IP failure rates between products. Adding a data structure specific to the failing IP block provides a standard and enables data sharing.

The remainder of this paper discusses in depth the framework to share data between Design, Fab, and Test engineering teams. Section II defines the design data of interest and describes a data structure to use in a test program. Next Section III describes the enterprise data architecture options. Section IV examines the benefits to the various engineering teams. The experiences in implementing this concept at a major IDM are shared in section V. The summary section, VI, includes a list of steps to enable the proposed framework.

II. Connectiing the Silos: Proposed Data Structures and Design Data to Share

Connecting the silos of Fab and Design data via Test data necessitates well designed data structures, data governance and a thoughtful integration into the existing enterprise architecture for this data. This section proposes the data structures and uses several IP blocks to illustrate the concepts.

IP blocks were chosen from the IP lists found at www.design-reuse.com and are used for illustrative purposes only. Following blocks were chosen:

- Soft IP MIPI Slave controller, from Cadence
- Soft IP USB 3.0 Device Controller from T2M
- Hard IP MIPI MIPI D-PHY 1.5 GBPS from Cadence
- Hard IP USB3 from OmniPhy

The IP data shared below is representative in nature and does not represent a real design.

A. *IP Identifier*

The IP Identifier, **key** data structure, ties test results to associated IP design data. A straightforward scheme would concatenate the IP name, configuration and vendor. IP Identifier format would be as follows and is illustrated in Table 1:

IPblockname_IPConfiguration_IPprovider

Note the format is not significantly different than TSMC IP Tagging specification[8].

Table 1 IP Identifier Format Examples

IP	IP Identifier
Soft IP1	MIPI Slave Controller_NA_Cadence
Soft IP2	USB3.0 Device Controller_NA_T2M
Hard IP3	MIPI D-PHY_1.5Gbps_Cadence
Hard IP4	USB3_6GTs_OmniPhy

B. *Essesntial IP Design Data*

When factory engineers have access to IP design data they can reduce the time to address yield issues and can rapidly ramp new product. The following essential data is required for both Soft and Hard IP:

- Device Types
- IP block dimensions: X, Y microns and assume square block
- SE corner location on the die, assume SE corner of die is 0,0 in X & Y, note assumes only 1 copy
- Layer, critical area

In addition, this essential data enhances interpretation of IP manufacturability rates. Table 2 summarizes representative data for two IP blocks.

As will be discussed in Section III, several storage mechanisms exist. If storing in one data structure, the design data is held in a substring of variable lengths separated by a semicolon, "**;**", and design data identifier starts the substring with followed by a colon, "**:**". Example:

```
DEVICE:nmos1,pmos1,LPnmos,LPpmos;
DIMENSION:100 x 200; LOCATION:
500,337; M1: 50; M2:60; M3 70.
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Table 2 Essential IP Design Data Examples

Design Attribute	Soft IP1	Hard IP4
Device Types	nmosl, pmosl, nmosll, pmosll	nmos, pmos, nmosl, pmosl
IP Dimension X, Y	80 x 135 um	170 x 110 um
SE corner location X, Y	500, 653 um	4500, 450 um
M1 critical area	863 um**2	1280 um**2
M2 critical area	547 um**2	788 um**2
M3 critical area	412 um**2	654 um**2

C. *Additional Design Data of Interest*

Deeper knowledge of an IP's design implementation can further aid Fab, Test and Design engineers. A Fab engineer might want to know the distribution of standard cells in an IP. While a design engineer might want to know the orientation of the IP within the design, # of copies used, synthesis strategy used by the SoC design team. IP identifier provides the link between the test results and a longer list of data. The examples of additional design data in Table 3 came from discussions with both Fab and IP design engineers at an established IDM. It is by no means an exhaustive list. As the list can become quite large it would be cost prohibitive to include all of this data in test data log. However, it would be worthwhile to maintain this data in an off-line table.

Table 3 Examples of Additional Design Data of Interest

Design Attribute	Example data
Standard Cell library	Low power Standard Cell library for TSMC 28nm
Standard Cell, # of occurrences in IP	StdcellA- 303, StdcellB- 112, etc.
# of instances in design and XY Location(s)	Instance 1(200um 468 um) Instance 2(500 um 480 um)
Data rates for a SERDES	6.0 GTS
Synthesis parameters: clock rate	125 Mhz
Hard IP, layout orientation NS vs EW	NS
Hard IP, Input reference clock	125 Mhz

The standard cell library choices provide insight to both the SoC integration companies and the IP developer. Several papers have highlighted the difference that a standard cell choice can have on manufacturability [9][10][11]. Synthesis strategies historically have focused on timing, power and die area, as noted

in [12], adding DFM metrics would assist in increasing yield. Techniques in synthesis to harden an RTL design against process variation could also be captured.

III. Connecting the Silos: Enterprise Data Architecture and Data Analysis

This section discusses the enterprise data architecture to support the framework for sharing data on IP manufacturability. In connecting knowledge silos one needs to consider factory automation system, test results, design data. Data analytic solutions can easily support dashboards and visualizations to enable analysis for IP manufacturability.

A. *Enterprise Architecture*

Currently most factory data automation systems have become complex enterprise systems because over time engineering teams add capabilities and requirements. In such scenarios, it is advised to use an existing underutilized data structure. With the redesign of test factory automation system companies have the option to simplify implementing a data system to support IP manufacturability. Both approaches will be explored.

The pathfinding work at the IDM discussed later (Section V) repurposed an underutilized 256-character existing data structure. This approach provided a means to clearly define the data structure and establish rules for data governance. The test program could then report out the IP causing the fail/downbin and the essential design data. Test engineers can place the essential data inside a module in the test program via a look-up table and store remaining data maintained in a separate data base. The latter data base can reside in either the Factory automation system or an accessible Design database.

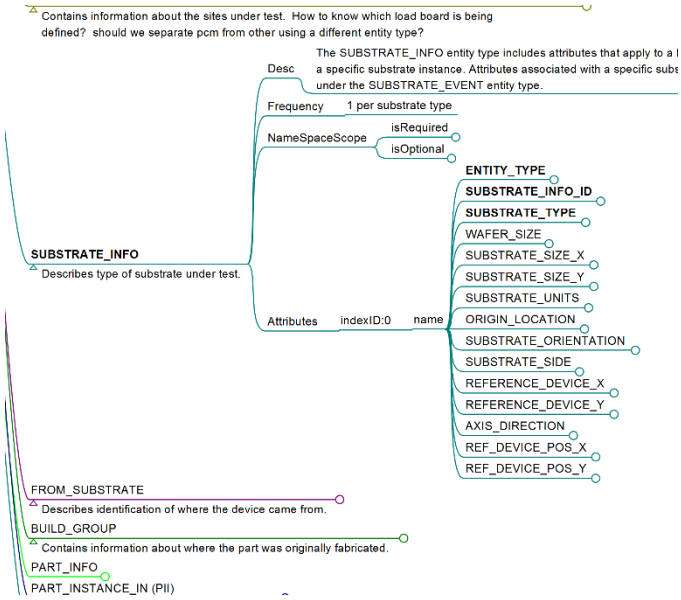

Figure 2 Substrate Info in RITdb Datalog

Engineering team redesigning factory automation systems can consider newly developed standards. The Semi CAST initiative (CAST-Collaborative-Alliance-Semiconductor-Test) Rich Interactive Test Database RITdb [15] offers a framework in which all design data could be held in a static table with the IP identifier as the key that connects IP results with the IP design data. The RITdb mind map describes the data architecture. The Substrate_info category, which describes the device under test (see Figure 2), seems ideal to support the IP design data. An engineer can add a list of IP for each device under test and then create a sub-tree which can hold the associated IP design data. The test program data log would report the IP Identifier and the additional data can be accessed off-line.

In both approaches the test program reports only a portion of the design data. The remaining design data resides in another database. The ability to connect data between the two separate systems presents a challenge to both IDMs and the Foundry eco-systems. The enterprise architect needs to assure:

- Access permission control administration exists,
- Good Information Quality [14] practices have been established,
- Design data has a single group maintaining the data; i.e. Master Data,
- Engineers know where to find and analyze the data.

B. *Enabled Data Analysis*

With IP manufacturability tracked at the factory level the ability to create IP-centric dashboards and trigger flags for IP manufacturability issues can be pursued. Several examples are shared and a brief discussion on current semiconductor manufacturing analysis software is included.

First, consider a simple Dashboard of IP manufacturability health. The metric of health could be simplistic in terms of % fails/performance hits or could be more realistic with respect to yield by noting the Si Area for the IP. Presuming several products running through the same Fab and using the IP's listed in Table 1 a Table 4 like can be used.

Table 4 IP Fail Rate in % of Fails

IP	Prod A	Prod B	Prod C	Prod D
Soft IP 1	.02%	.05%	.03%	.05%
Soft IP 2	.04%	.05%	.03%	.04%
Hard IP 1	.10%	.12%	.24%	.15%
Hard IP2	.23%	.48%	.23%	.24%

Another popular means of comprehending yield issues is a pareto chart. Typically, these are for Failure type (leakage, delay faults), with IP monitoring the graph in Figure 3 becomes possible. With the subtle interaction between design and fabrication at the advanced nodes, engineering teams would benefit from seeing an issue sooner. Aggregating failures of an IP across multiple products enables such a capability. Development of such a metric requires a thoughtful implementation and is an area of future work.

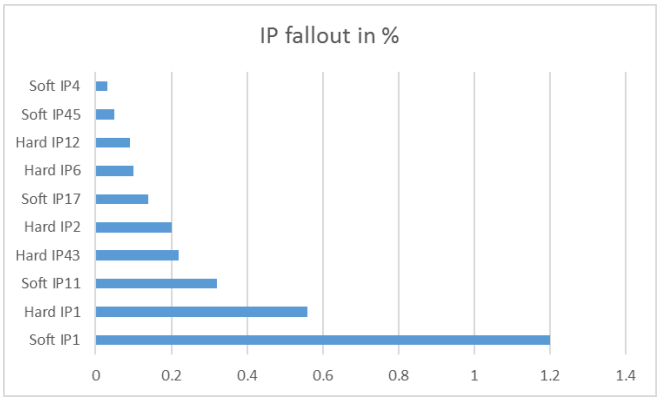

Figure 3 IP Paretos

Eight companies offer a variety of data analytic tools for IDMs and Foundry Eco-system players to gain insights into the manufacturability of semiconductor products. Adding IP manufacturability metrics and the additional data could be easily supported. As one vendor stated, "It's a few more data types." The eight companies and their associated analytic platforms include:

- BisTel- Yield Map Analyzer
- D R Yield- YieldWatchDog
- Galaxy- Yield-Man™
- Mentor Graphics- Tessent YieldInsight
- Optimal Plus- Yield+
- PDF Solutions- Exensio-Yield™
- Qualterra- Silcondash
- Synopsys-Yield Explorer

IV. Benefits to the SoC Eco-System Partners

The proposed framework for IP manufacturability benefits the Fab/Design Integrator/IP designer eco-system. In an IDM as well the Foundry eco-system Fab, Test, SoC Design and IP Design organizations operate as siloed organizations. Increasing data sharing between the engineering teams results in the ability to respond sooner to manufacturability issues and in an increased understanding of manufacturability of an IP. In the next few paragraphs the benefits for each engineering team will be discussed independent of eco-system type. The differences between how these benefits would manifest itself in an IDM vs the Foundry eco-system will then be addressed.

For the Factory (Fab, Assembly & Test) having essential IP design data reported out with IP fails/performance degradation aids in the deciphering manufacturability issues. IPs are used in multiple products in a Fab. Aggregating the yield data for an IP across multiple products gives the factory yield engineer the ability to observe a common issue sooner. A Test engineer will be interested in understanding fallout results per IP and the ability to compare IP pareto across products. Having essential design data easily combined with test program results assist with triage of causation for yield/performance loss. More detailed design data available in a second/offline database can greatly assist in the determination of yield/performance losses. It also enables an engineer to determine if differences between an IP's yield across different products is due to design implementation differences. Yield and test engineering teams provide the IP yield and design data to the design teams to educate.

For the SoC design team increasing a products manufacturability has an impact on profitability for this product. Having access to IP failure rates SoC design teams can be informed on how IP implementation choices that could impact manufacturability. With access to IP manufacturability data an SoC design team can be informed about potential issues for products which reuse IP. IP reuse numbers reported in [1][2] can be found in the Table 5. Note reuse numbers are relative to the previous product. Currently usage of IP across products remains unknown; understanding IP utilization would assist in assessing the value of the framework proposed.

Table 5 IP Reuse numbers

Eco-system	Reuse in Revised Designs	Reuse in New Product Designs
IDM	73%	44%
Foundry based	64%	44%

For Soft IP a SoC design team may have different standard cell libraries to choose from and have synthesis choices that impact manufacturability [12]. Matching the design data in the secondary data base with the Factory data could inform choices on the next implementation and even perhaps the overall strategy. True SoC designs enable the quick turnaround of a design due to the disciplined usage of a connection fabric like SONICs. If the yield loss causation points to revising the IP design, then the ROI analysis can be done to determine if the cost of a design turn will benefit the profitability.

The IP design team resides furthest removed from manufacturability issues both physically and philosophically. The latter is a result of the evaluation of IP in terms of ease of design integration. The Quality Intellectual Property Metric, IEEE 1734, focuses on documentation, ease of integration, design & verification Quality. Not a single check box for manufacturability exists in that standard. Standards to address the manufacturability have been limited to foundry IP qualification [13]. For the proposed framework to share data, IP design teams play a crucial role. While performance and ease of integration primarily dictate the choice of an IP in an SoC design the ability to get product to market is the ultimate proving ground for any Si design. Providing design data to their SoC design and Factory partners adds to their value as a part of the eco-system. The proposed framework to share data can provide feedback in particular for Hard IP designers. Hard IP reuse sometimes has subtle differences between "identical" IP that could impact manufacturability. For instance the reference clock into a USB block can differ from one product to another.

The differences between the IDM and the Fabless eco-systems may impact the ability of placing design data at a

factory engineer's disposable and enabling designers (SoC and IP) insight into an IP's manufacturability. The differences lie primarily in the business transactions in the Foundry eco-systems. In the IDM system no financial boundaries exist, albeit there remain the organization boundaries that form the foundation of the knowledge silos. For the Fabless eco-system, the business transactions come into to play but are not insurmountable.

Foundries provide Fab services and offer IP to their customers. In addition, they have different levels of partnership's with IP vendors. Some are considered Prime partners which warrant a closer collaboration on the IP development. Let's assume that for the purpose of this paper that even with this closer collaboration that IP yield is not generally made available to IP providers. Foundries have an opportunity to financially benefit from comprehending IP manufacturability in the following ways:

- They can improve the yield of their developed IP thereby making them more attractive.
- They can compare the IP yield across multiple SoC designs and create an IP manufacturability metric.
    - SoC design companies would purchase to guide IP usage.
    - IP design companies would purchase for understanding their product and potentially their competitors.
- They can provide IP metrics to their customers.

SoC design companies choose either purchasing a wafer or Known Good Die (KGD) from Foundries. For wafer purchase manufacturability issues become a financial interest of the SoC design company. To effectively respond to yield issues, SoC design companies can successfully partner with Foundries and OSAT by enabling IP monitoring in the test program and by providing IP design data. Such data sharing would require additional contract obligations. With a KGD purchase the Foundry bears the yield loss burden. Via contract Foundries can require IP design data and test program monitoring of IP fails to enable faster yield improvement.

V. Implementation Challenges

This section shares observations from Intel pathfinding work on two products, 32nm and 22nm process nodes respectively. For the pathfinding work the team focused on providing the essential design data. Overall the team found the actual reporting of the data for a failing IP to be straightforward. Acquiring the design data per IP proved to be more difficult than expected. Implementing a new methodology uncovers some challenges. In the Intel case, none of the challenges were showstoppers.

A. Inability to Uniquely Identify Which IP block Caused the Failure

The pathfinding studies showed that the actual reporting of data for a failing part was straight forward. Identifying the failing IP was sometimes confounded by the scan-chain implementation or the nature of a functional test touching multiple IP blocks. To handle this scenario, the team chose to report out both IP blocks as part of the fail along with their essential design data. As SoC design companies have different design practices and interconnection buses such situations may not occur.

B. Inconsisent Test Data

In the first pilot, the wafer test engineer supported initial test program development for IP identification. The engineer's code provided the ability to identify and report out the failing IP failed. The unit test engineer adopted this code. However, differences existed in the exact data string reported out. Thus making it a challenge to compare wafer and unit level test results. This data governance issue could be avoided with an agreed upon data string format. The second pilot also showed a difference between wafer and unit testing. The wafer test engineer committed to reporting out the failing IP and the essential design data. However, the unit test engineer would only commit to reporting out the failing IP. A way to handle this would be to have clearly stated test program requirements that included the need to match data between wafer and unit level testing. Another option is to have all design data in an offline data base that the IP identifier could be used to access. Using the CAST RITdb enables such an option which simplifies the test program requirements.

C. Inability to Aquire IP Design Data

In the 32nm pilot, the team met several obstacles with their inquiries for requested design data. The data existed somewhere in the design data systems but it seemed a challenge to find the right engineer to get the data. This was more of a challenge for the Soft IP than the Hard IP. The team identified this situation as a lack of centralization of the data per IP. Various spreadsheets were manually compiled by engineering teams in the IP design organizations. At the product level engineering teams manually created spreadsheets. This began to change as the team prepared for the 22nm pilot as we learned of a database for tracking IP/SoC decisions [16]. The team informed the database architect of IP manufacturability needs. In return, the IP failure rate could be feedback back to the design teams via their data base. None the less acquiring design data remained a manual process for the 22nm pilot.

A commitment to provide the design data needs to be made by both the SoC design team and the IP design teams. The manufacturing team can document the requested design data and the required format. A negotiation may follow in which only a portion of the data is provided. While not ideal, it offers a start at connecting data across the knowledge silos.

D. Inconsisent Design Data per IP

Manually tracking IP design data makes it prone to errors. Add to this multiple engineering teams manually tracking data can result in inconsistent data, i.e. the spreadsheets don't match. The team found that transistor types in an IP block were reliably tracked; however, IP area was inconsistent between sources. During the 22nm pilot the team learned that there existed an engineering team that was automating producing a spreadsheet that had very detailed data for Hard IP. This held promise in that it would put into practice Master Data concepts [17].

In a Master Data framework **one team** maintains the data for the whole company. While this centralized Hard IP engineering team had only begun this work, i.e. at the pilot stage, they became the defacto Master Data owners for Hard IP design data. Soft IP lacked anyone owning the Master Data role. As they track Soft IP product utilization Soft IP program managers would seem a natural choice due to their centralized role. However, SoC design team synthesize the Soft IP and connect it to the product. Identifying engineers on the SoC design team to be the Master data owners for their product represents a more practical choice.

E. Traceability of IP Names

The team assumed that the IP names in the IP data bases would be the same in the SoC design. Unfortunately, this assumption turned out false. As the wafer and unit test programs used the SoC IP design names, the team had to map the names to enable design data. For the 32nm pilot provided only the IP name. For the 22nm pilot a team member constructed a spreadsheet that mapped the design data to IP name used by test.

The enterprise architect team member eventually determined the design practices that resulted in name changes. Two plausible solutions exist. The first is simple- don't change the IP name when integrated into the SoC design. Second- presuming that name modifications are inevitable track the name changes and provide a decoder ring between the IP block name and its SoC design name.

F. IDM versus Foundry Eco-system Considerations

The experiences described in this section come from one IDM's exploration in joining formerly disparate knowledge silos. From an engineering perspective, this author sees no distinct difference from the IDM eco-system and the Foundry eco-system when attempting to join these knowledge silos. Barriers to joining these silos exist and include: corporate organization, implementation and technical barriers. These barriers can be overcome with commitment and standardization. The difference between the IDM and Foundry eco-systems relate to the additional business relationships which the latter system needs to accommodate. As discussed in Section IV the businesses can add the IP data requirements to their contracts with each other.

VI. SUMMARY

In a SoC design eco-system IP reuse provides faster product to the Fab. To enable a correspondingly faster product ramp semiconductor manufacturing data analysis needs to shift from a *product* to an *IP* viewpoint. Connecting the knowledge silos of Design, Fab and Test with relevant IP design data enables multiple engineering teams to be more efficient and innovative. This paper presented a framework to monitor IP manufacturability and to provide IP design data. This design data can augment existing data analytic tools which can then enable disparate engineering teams to share insights with each other. The paper thoroughly discussed the value in comprehending manufacturability at the IP level has to Design, Fab and Test engineering teams. The author shared experiences piloting these ideas at an IDM which revealed implementation challenges, none were show stoppers.

To move forward on making this a reality the following steps are required:

- Define the IP design data parameters to include per IP. As necessary separating into essential and in-depth.
- Determine ownership of suppling the design parameters, i.e. SoC integrator and/or IP vendor.
- Assign a Master Data team to own keeping **one true record** that engineering teams can rely upon.
- Establish a data base organization which includes data structures, data governance. CAST's RTdbi proposal could easily support needs.
- Address the traceability of IP names from IP Design to SoC Design to Test Program.
- Create the Test Program to support IP fail/performance hit report outs.
- Use the data to support manufacturability issues and report IP fail rates to design teams.
- Enable Data Analysis and Visualization options.

Manufacturing and Design organization have silos of expertise and knowledge; joining these knowledge bases have both organizational, implementation and technical barriers. The ultimate gains outweigh the effort. With the proposed data sharing framework Jane would not have wasted 100 hours of engineering time chasing the incorrect transistor to address an IP yield issue.

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