ANNE MEIXNER PHD

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SENIOR SEMICONDUCTOR TEST ENGINEER

FLUENT IN DIGITAL, MEMORY, MIXED-SIGNAL AND ANALOG TEST AND DFT

Dynamic Technical Leader delivering cost saving test methods for products on advanced technologies. Effectively proves new test methods which lower manufacturing test cost with empirical data and drives adoption via presentations, documentation and training. Successfully applies collaboration skills- connecting people and connecting knowledge across engineering teams. Core strengths include:

Defect Based Testing • Design for Test (DFT) • Interface (I/O) Test • Analog Test • Memory Test • Process Variation • Wafer & Final Test • Data & Statistical Analysis • Design of Experiments • Data System Improvements • Cross-functional Team Collaboration • Technical Program Management • Training Development • Requirements & Specification Writing • Standardizing Methods/Processes • Communication • Mentoring & Coaching.

Strength Finder 2.0: Responsibility • Activator • Achiever • Learner • Woo

Professional Overview

Test Engineer Consultant and Engineer Coach

The Engineers' Daughter LLC Portland OR 2015-present

Engineering Consulting and Engineer Career Development

- Consulting editor at Semiengineering.com with monthly articles on analytics in the semiconductor industry.
- Customer Solutions Consultant for Teseda-- technical sales to new and existing customers. Teseda provides silicon debug and defect isolation solutions which leverage scan technology.
- Provided expert advice at a test engineering quarterly review for Cypress Semiconductor, 2016.
- Published and presented four technical papers/posters on the topic of IP manufacturability: 2016 Defects Adaptive Test, Yield and Data Analysis (DATA) Workshop, December 2016 Design and Reuse IP-SoC Conference, 2017 Advanced Semiconductor Manufacturing Conference, 2017 International Test Conference.
- Corporate training for engineer professional development. Recent clients include Intel, Boeing.
- Talks at professional development conferences: "Demystifying the Corporate Technical Ladder," "Getting To Present," "Presenting Technical Content with Confidence," "Engineering Presentations: Up the Engagement," "Creativity Habits for Everyday Engineering."
- Writing about engineering: engineersdaughter.org- a site for engineering stories, "Testing 1 2 3" articles at accendoreliability.com June 2017-Sept 2017. Collecting engineering stories from others, project described at Forum on Philosophy Engineering and Technology 2018 in talk "A Thousand and One Engineering Stories."

Electrical Validation (EV) Engineer

System Validation Engineering Intel Corp Hillsboro OR 2013-2015

Liaison between EV and Manufacturing Test.

- Led an engineering team to define a Converged Unit Selection Methodology to support first silicon validation.
- Defined standard forum and technical process for using carefully selected units.
- Chaired part selection forum for a 14nm product. Chose a software tool to improve timely part selection. Q1 2015 division award.

Contributed to Lab Efficiency Team's strategic vision of data system tool integration for non-manufacturing labs (~1500).

- Prioritized improvements by conducting in-depth interviews with 19 lab managers. Summarized results and presented to decision makers.
- Led Information Quality surveys on 3 key data systems to guide improvements.

Test R&D Engineer

Sort Test Technology Development Intel Corp Hillsboro OR 1994-2013

Responsible for new test methodologies that impacted product manufacturing test flows and lowered costs. Pursued defect-based test methodologies which often relied upon new DFT circuitry. Conducted pathfinding work on test methods for analog circuitry. Direct contributions to bringing cost saving test technologies to products in a high volume manufacturing test environment for analog, I/O and memory circuitry. Effectively proliferated new methods via presentation, documentation and training. Mentored junior engineers. Led cross-functional teams to deliver new test methods and to share learnings across product teams. Strategic vision demonstrated with identifying test method needs and defining IP HVM tracking to support SOC. Proactive technical leader advocating mentoring of others via formation of Oregon Technical Leadership Forum.

Key contributions include:

- Designed 1st Weak Write Test Mode (WWTM) circuit and proved efficacy. Developed qualification plan, performed

data analysis from test programs and failure characterization, and proliferated the method via internal conference papers, internal documentation and training presentation. WWTM substituted the data retention test which significantly impacted test time (~100 us vs 1 sec). Technology successfully used for 10 years.

- Participated in Memory Test Methods Joint Engineering Team which focused on improving and standardizing embedded memory test methods. Wrote up DFT based test methods for internal test methods handbook—key reference for product development engineering teams. Contributed to memory test audit checklist and participated in several audits. Team awarded an internal award.
- Validated AC IO Loopback DFT on Willamette, 1st CPU to use this method. Analyzed AC IO loopback silicon data and provided input to establish fail limits. Proliferated the methodology via documentation and training. Technology continues to be used on nearly all Intel single-ended interfaces, i.e. DDR.
- Led pathfinding on High Speed IO test method development. Executed Inductive Fault Analysis (IFA) on key circuits. With designers defined DFT and directed Pre-Si DFT validation for PCI Express & Scidlink MI. Effort identified issues, work-arounds and improvements. Results communicated to Test engineer, DFT and IO design communities via presentation and documentation.
- Influenced DFT definition for QPI and FBD HSIOs by documenting requirements in QPI and FBD specs. Drove IO DFX definition for CPU tech focused on loopback, slow speed and no-touch test leakage. Defined and directed DFT implementation for QPI on test chip. DFT included slow speed operation and no-touch test leakage. Developed QPI Interface requirement for ATE vendors.
- Defined and directed pathfinding projects for HSIO RX equalization and RX Data Clock Recovery. Projects defined and directed engineers to complete the study. Work identified gaps and proposed test strategies for coverage.
- Led development of two courses on Intel IO DFT based test methods (Basics and Theory and Practice) by forming an instructor team. Drove a major update of material in 2008. Supported creating Web Based Training of Basics class. Trained additional instructors and gave training to 100’s of engineers.
- Led a remote cross-functional engineering team in a major revision of I/O test methods chapter.
- Co-chaired IO DFT and Test Joint Engineering team for 6 years. Responsible for agenda, meeting facilitation and SharePoint site organization to promote company-wide sharing of techniques and application.
- Executed a study on IO test fallout for multiple products during a fixed time period to comprehend fallout trends, test times in context with overall fallout and product test costs.
- Participated in SOC DFT & HVM WG and drove Analog/IO Testing strategy. Collaborated with Hard IP DFX engineers to develop IO DFX standards which addressed test infrastructure, basic requirements and staffing model. Conducted an extensive competitive analysis on IO and Analog test within SOCs.
- Defined Intel funding for academic research in PLL DFX and led a 4-year relationship between Intel engineers and research group. Via internship research applied to 22nm PLL design. Results shared in papers.
- Led Tooling and DFT Technology Working Group to develop and promote DFT test methods which support simpler load board designs. With WG members made a strong case for the No Touch Test (NTT) methods that would support increasing parallel test on future CPUs for 22nm+. Directed execution of experiments on new and existing No Touch Leakage methods. Led WG to document current tooling configurations and implementation trends for unit and wafer level test.
- Identified need to track IP HVM performance to support Intel’s SoC products. Gathered experts to define and executed a proof of concept on 32nm products. POC confirmed that with appropriate DFT architecture testing can easily support identifying failing IP. Identified acquiring the IP design data as in issue. Pilot on 22 nm product done which highlighted challenges in mapping the IP design data to tested IP.
- Conceived a monthly forum for sharing tips and ideas on technical leadership which also fosters informal networking. The Oregon Technical Leadership Forum successfully hosted 10 monthly forums for 5 years.

Graduate Research Assistant, PhD Student
Electrical and Computer Engineering, Carnegie Mellon University, Pittsburg PA 1988-1993
Developed a general methodology for analog fault model development, implemented for CMOS op amps. Designed op amps covering a range of topologies. Evaluated the effects of shorts on CMOS op amp behaviors. Wrote PERL code to post-process results and created circuit simulation input files for further analysis. Executed simulation experiments to determine resulting fault behaviors.

Associate Engineer
Product Assurance, IBM East Fishkill NY 1985-1988
Performance evaluation of logic gate array designs for high end computers. Training in Scan Test based upon LSSD technology, including diagnostic CAD tools. Evaluated via empirical experiments first Weighted Random Pattern test application at IBM (Pre-cursor to Logic BIST using weighted random patterns.)

Patents, Awards, Publications, Technical Activities:

Patents

5,559,145: “Static Random Access Memory SRAM Having Weak Write Test Circuit”

6,477,674: “Method and Apparatus for Conducting Input/Output Loop Back Tests Using a Local Pattern Generator and Delay Elements”

7,019,550: “Leakage Testing For Differential Signal Transceiver”

Awards
2003 International Test Conference Best Paper
2001 Intel Design and Test Technology Conference Best Paper
1995 Intel Design and Test Technology Conference Best Paper
1996 International Test Conference Best Paper

Publications
External publications only.
2017 Advanced Semiconductor Manufacturing Conference: “Enhancing Yield Learning on SoC Designs by Tracking IP Manufacturability”
2016 Design and Reuse IP-SoC Conference: “A Knowledge Sharing Framework for Fabs, SoC Design Houses and IP Vendors”
2016 DATA Workshop: “Improved Understanding of IP Manufacturability—A Proposal to Share Data between Fab, Test and Design”
2013 VLSI Test Symposium: “Universal IDDQ BIST Approach to Characterize a Phase-Locked Loop Parameters.”
2012 Design and Technology of Integrated Systems Conference: “Improving IO Test and System Evaluation via Data Sharing.”
2011 International Test Conference: “Signal Integrity Considerations for System Test for High Speed IOs” poster
2011 VLSI Test Symposium: “Challenges in High Volume Manufacturing Test of HSIO and Correlation to System Performance” invited industrial talk
2011 VLSI Test Symposium: “An Industrial Case Study of Analog Fault Modeling “
2008 International Test Conference: “External Loopback Testing Experiences with High Speed Serial Interfaces”
2007 Mixed Signal Test Workshop, “Gaps in Timing Margining Test for Serial Interfaces: A Case Study”
2004 Custom Integrated Circuit Conference, “Design Considerations and DFT to Enable Testing of Digital Interfaces”
2004 IEEE Design and Test of Computers: “Testing Gbps Interfaces without a Gigahertz Tester”
2003 International Test Conference: “Elimination of Traditional Functional Testing of Interface Timings at Intel”
2003 VLSI Test Symposium: “Don’t Touch Those Pins! Manufacturing Test for High Speed Serial (HSS) Interfaces” invited industrial talk
1996 International Test Conference: “Weak Write Test Mode: An SRAM Cell Stability Design for Test Technique”
1991 International Test Conference: “Fault Modeling for the Testing of Mixed Integrated Circuits.”

~12 internal publications at Intel Conferences

Technical Activities
IEEE Member since 1994
International Test Conference Program Committee 2000-2004
DATA Workshop 2016-2017 Panel Organizer
P1687.2 (Analog Test Access)- and P2472 (Analog Test Coverage) standards committee; editor for P2472
SRC Liaison for Prof Sule Ozev, AZ State University on analog fault modeling methods for test coverage and yield
Intel Research Liaison for Prof Martin Margala, University of Massachusetts Lowell on PLL DFX research

EDUCATION

PhD in Electrical and Computer Engineering; Carnegie Mellon University

MS Electrical Engineering; New York University

BS Electrical Engineering; University of Maryland

OTHER RELEVANT EXPERIENCE

Professional Ski Instructor of America (PSIA) for 22 winter seasons at Mt Hood Meadows; Certification Alpine II

Hollywood Farmers Market volunteer since 1997: responsibilities- greet, crowd counts, and assist single vendors.