Anne Meixner
Phd

Patents and Publications

Throughout her engineering career Anne has shared technology results and proposals at engineering conferences. The majority of these publications are available via IEEE's Digital Library.

2017 Advanced Semiconductor Manufacturing Conference: "Enhancing Yield Learning on SoC Designs by Tracking IP Manufacturability"
https://ieeexplore.ieee.org/document/7969210
2018- International Test conference: What's up with Analog Test Coverage: IEEE P2427 IEEE Working Group Progress (poster)
2017- International Test Conference: An Immodest Proposal to Bridge Test and Design Data for SoC and IP Yield (poster)
2017 Advanced Semiconductor Manufacturing Conference: "Enhancing Yield Learning on SoC Designs by Tracking IP Manufacturability"
https://ieeexplore.ieee.org/document/7969210
2016 Design and Reuse IP-SoC Conference: "A Knowledge Sharing Framework for Fabs, SoC Design Houses and IP Vendors"
https://www.design-reuse.com/articles/41315/knowledge-sharing-framework-fabs-soc-design-houses-ip-vendors.html
2016 DATA Workshop: "Improved Understanding of IP Manufacturability—A Proposal to Share Data between Fab, Test and Design"
(link to downloadable version of paper- Final Ameixner-IP...DATA 2016)
2013 VLSI Test Symposium: "Universal IDDQ BIST Approach to Characterize a Phase-Locked Loop Parameters."
https://ieeexplore.ieee.org/document/6548911
2012 Design and Technology of Integrated Systems Conference: "Improving IO Test and System Evaluation via Data Sharing."
https://ieeexplore.ieee.org/document/6232967
2011 International Test Conference: "Signal Integrity Considerations for System Test for High Speed IOs" poster
2011 VLSI Test Symposium: "Challenges in High Volume Manufacturing Test of HSIO and Correlation to System Performance" invited industrial talk
2011 VLSI Test Symposium: "An Industrial Case Study of Analog Fault Modeling"
https://ieeexplore.ieee.org/document/5783780
2008 International Test Conference: "External Loopback Testing Experiences with High Speed Serial Interfaces"
https://ieeexplore.ieee.org/document/4700557

2007 Mixed Signal Test Workshop, “Gaps in Timing Margining Test for Serial Interfaces: A Case Study”
2004 Custom Integrated Circuit Conference, “Design Considerations and DFT to Enable Testing of Digital Interfaces”
https://ieeexplore.ieee.org/document/1358776
2004 IEEE Design and Test of Computers: “Testing Gbps Interfaces without a Gigahertz Tester”
https://ieeexplore.ieee.org/document/1316774
2003 International Test Conference: “Elimination of Traditional Functional Testing of Interface Timings at Intel” **BEST PAPER**
https://ieeexplore.ieee.org/document/1271089
2003 VLSI Test Symposium: “Don’t Touch Those Pins! Manufacturing Test for High Speed Serial (HSS) Interfaces” invited industrial talk
1996 International Test Conference: “Weak Write Test Mode: An SRAM Cell Stability Design for Test Technique” **BEST PAPER**
https://ieeexplore.ieee.org/document/556976
1991 International Test Conference: “Fault Modeling for the Testing of Mixed Integrated Circuits”
https://ieeexplore.ieee.org/document/519719

Note IEEE publications reside behind a paywall, though you can read the abstract. DATA workshop paper has been provided. Contact me here if you are interested in the associated presentations.

Anne holds three US patents in the area of semiconductor testing.
5,559,145: “Static Random Access Memory SRAM Having Weak Write Test Circuit”
6,477,674: “Method and Apparatus for Conducting Input/Output Loop Back Tests Using a Local Pattern Generator and Delay Elements”
7,019,550: “Leakage Testing For Differential Signal Transceiver”